ABSTRACT

A system and method to provide memory test patterns for the calibration of a delay locked loop (DLL) using a pseudo random bit sequence (PRBS) stored in a serial presence detect (SPD) circuit memory. The test bits stored in the SPD memory are transferred to a memory controller register (MCR) and implemented on the system data bus as test patterns that closely simulate run-time switching conditions on the system bus, so as to allow more accurate calibration of the DLL. Test data write/read operations may be performed while signals for the test patterns are present on various bit lines in the data bus so as to allow for accurate determination or adjustment of the value for the delay to be provided by the DLL to the strobe signals during memory data reading operations at run time. Memory chips may also be tested over an operating range of values using the generated test patterns.